ECE 2020-IE1

Fundamentals of Digital Systems Design

Spring 2026

Meeting Days, Time & Location: MW 11:00–12:15 PM, Van Leer C241

Instructor: Niyem Bawana
Email: bawana@gatech.edu
Office Hours: MW 5:00–6:00 PM via teams (Click to Join ECE2020-IE1 Office Hours) or by appointment
TA: Somujayabalan Saathvik, Office Hours: Tuesdays 2:30 PM–4:30 PM and Thursdays 10:30 AM–12:30 PM Location : TBD

Course Description

ECE 2020 introduces the many levels of abstraction that enable today's digital systems. It explores digital design at the layers from switches and wire to a programmable machine. At each layer, the design process of transforming a specification into an implementation is introduced and practiced.

Course Objectives and Outcomes

- **Analyze and implement** Boolean logic functions using truth tables, logic schematics, and algebraic representations.
- **Evaluate and analyze** physical implementations of digital logic, including CMOS-based circuits, with particular emphasis on timing behavior and performance trade-offs.
- **Apply and manipulate** number representations used in digital systems, including binary, signed, and fractional formats.
- **Design and construct** combinational digital subsystems using fundamental building blocks such as multiplexers, decoders, and encoders.
- **Design, implement, and analyze** sequential logic systems, including digital storage elements and finite state machines, to realize specified system behaviors.
- **Explain and apply** basic processor architecture concepts and **develop** simple assembly-language programs to demonstrate processor operation.

Course Materials

- Wakerly, *Digital Design: Principles and Practice*, 5th Edition
- Wakerly, *Digital Design: Principles and Practice*, 4th Edition
- Harris & Harris, *Digital Design and Computer Architecture* (available through library)

Course Websites:

- New Website: http://ece2020.ece.gatech.edu/new/
- Old Website: http://ece2020.ece.gatech.edu/

Grades and Assignments

Grade Distribution

Assessment Component	Weight
Final Exam	31%
Three Tests (14% each)	42%
Homework	7%
Two Labs (5% each)	10%
Mini Project	10%
Total	**100%**

Grading Scale

Letter grades: A $\geq$ 90.0%, B $\geq$ 80.0%, C $\geq$ 70.0%, D $\geq$ 60.0%

Guided Mini Project (10%)

Students will complete a small-group project (teams of 2–3) applying core concepts from the course. The project is intended to connect course material to students' motivations for enrolling in ECE 2020.

Project Categories

- **Option A: Combinational Logic System** - Design and analyze a digital subsystem using combinational logic.
- **Option B: Sequential Logic / FSM** - Design and implement a finite state machine for a real-world control problem.
- **Option C: Processor or Datapath Concept** - Develop a simplified datapath or processor concept and demonstrate operation via example instructions.

The project categories listed above are intended as guiding examples rather than restrictions; students are encouraged to propose their own project ideas aligned with course concepts, provided the scope is reasonable and the project is achievable within the semester timeline. All projects must be approved through the proposal submission before work begins.

Project Timeline and Deliverables

- **Project Proposal** (1 page) –Due 01/28/2026
  - Team members and project selection
  - Brief description of proposed design and objectives
- **Mid-Progress Report** (1–2 pages) –Due 03/09/2026
  - Initial design with diagrams/schematics

  - Preliminary results or calculations
  - Challenges and proposed solutions

- **Final Deliverables** –Due 04/06/2026
  - Final design report (2–3 pages)
  - Recorded video presentation (3–4 minutes maximum), with active participation from all team members. The presentation must be based on narrated presentation slides (PowerPoint, Google Slides, or equivalent).

Simulation-based tools are sufficient; no hardware is required.

Late Submission Policy

Homework: If unexcused, cannot be submitted late. Complete homework well before the deadline so that any issues can be fixed before it's too late. Email me with excused delays to work out submission details.

Participation: With a valid excuse, the grade will be dropped from the grade calculation. Assignments missed without a valid excuse will be a 0.

Tests: With a valid excuse, tests can be made up for full credit as soon as possible. Tests missed without a valid excuse can be made up as soon as possible with a penalty of up to 20% per day (adjusted based on ability to make up the test). Make-up tests may be different than the original and might not receive the same curve.

Labs: Labs are due one week after the in-class period. If the in-class portion is missed or is not completed within the lecture period, the lab must be finished outside of lecture. Late submissions will not be accepted beyond the one-week period.

Accommodations for Students with Disabilities

If you are a student with learning needs that require special accommodation, contact the Office of Disability Services at (404) 894-2563 or `http://disabilityservices.gatech.edu/` as soon as possible to make an appointment to discuss your special needs and to obtain an accommodations letter. Please also e-mail me as soon as possible to set up a time to discuss your learning needs.

Grade Disputes

Requests to regrade any assignment must be made within one week of the assignment being returned. In the event of a regrade, the entire assignment may be regraded.

Communication

Piazza for Technical Questions:

There will be a Piazza section set up and linked to Canvas. That is the preferred place to ask technical questions so that everyone in the class can see the answer (or answer themselves) and ask follow-up questions in the same place.

Before posting a new question on Piazza:

- Review existing discussion threads first; if someone has already asked your question, read through the responses.
- If you need clarification on an existing thread, reply to that thread instead of starting a new post.
- This keeps discussions organized and helps everyone find answers more easily.

Contacting the Instructor:

The best way to reach out to me is via email or through Canvas messages. If you need to contact me for non-technical reasons (course logistics, scheduling meetings, personal matters, etc.), I prefer email, but it is also possible to message me through Canvas. If I need to contact you personally, I will use your GT email address.

Course Announcements:

Announcements will be sent through Canvas. You are responsible for information sent in those announcements, so I recommend configuring Canvas to notify you of them.

Academic Honesty

At Georgia Tech, we believe that it is important to strive for an atmosphere of mutual respect, acknowledgement, and responsibility between faculty members and the student body. See http://www.catalog.gatech.edu/rules/22/ for an articulation of some basic expectations that you can have of me and that I have of you. In the end, simple respect for knowledge, hard work, and cordial interactions will help build the environment we seek. Therefore, I encourage you to remain committed to the ideals of Georgia Tech while in this class.

You May NOT:

- Collaborate at all during tests and in-class quizzes, unless otherwise specified.
- Share solutions to any assignment before its due date.
- Discuss tests until they have been returned, in case someone has not taken it yet.
- Use or reference lab work from previous semesters.

You MAY:

- Collaborate on homework, as long as solutions are not shared.
- Use previous semesters' exams, homeworks, or other resources from the general 2020 website, or from other sources.
- Use CAD or simulation software such as http://lushprojects.com/circuitjs/circuitjs.html.

Important Notes:

- Final Exams are scheduled by the Registrar and should not be duplicated on course schedules in case they change.
- Find the "final exam matrix" for the current semester to ensure that you always have correct exam schedule.

Course Schedule

Note: All topics and dates might change; pay attention to Canvas and watch for announcements.

Week	Topics	Wakerly 4th	Wakerly 5th	Wills&Wills	Harris&Harris
11-Jan	Class logistics and introduction	1.2, 1.4	1.2, 1.4		1.1-1.3, 2.1
	Boolean logic and expressions	4.0-4.1	3.0-3.1	BA	2.2
	Switches and switch networks	3.1		SW	
18-Jan	(Monday Holiday)				
	Algebraic manipulation and simplification	4.1			2.3
25-Jan	Transistors, logic levels, CMOS	3.3	1.9, 14.1-2		1.6, 1.7
	Gate-level design	1.3, 3.1, 4.2, 6.1.2, 6.1.7	1.5, 3.2, 4.1.2	GD	1.4, 2.4
	Mixed-logic notation and manipulation	4.3.2, 6.1.3-5	3.3.2, 4.1.3-6	GD	2.5
1-Feb	Logic simplification with K-maps & SoP	2.11, 4.1.6, 4.3.3-5	2.11, 3.3.3	BA, SP	2.2.2, 2.7
	Circuit timing	3.6, 4.4, 6.2	3.4, 4.2, 14.4		2.9
	Lab 1: Combinational circuits	1.6, 3.2, 3.4-5	1.7		
8-Feb	Number systems (representation, bases, math)	2.0-2.4	2.0-2.3	NS, AR	1.4, 5.3
	Number systems (negatives, fractions)	2.5-2.7	2.4-2.7	NS	
15-Feb	Test 1: Digital logic and implementation				

Course Schedule (continued)

Week	Topics	Wakerly 4th	Wakerly 5th	Wills&Wills	Harris&Harris
15-Feb	Building blocks, adders, subtractors	6.1.1, 6.1.8, 6.10	6.1, 4.1.1, 4.1.8-9, 8.1		5.2
	Encoders, decoders, implementation and uses	6.4, 6.5	6.3	BB	
22-Feb	Muxes, demuxes, implementation and uses	3.7.1, 3.7.3, 6.7	6.4, 7.1	BB	1.7.7, 2.8.1-2
	Latches & Flip-flops	7.0-7.2	10.1-10.2	LR	3.2
1-Mar	Finite state machines	7.3-4	9.1, 9.5		3.1, 3.4
	Designing FSM behavior	7.5			
	Test 2: Numbers, Building blocks				
8-Mar	Physical FSM implementation	7.6-7.7	9.3		
	FSM architectures				
15-Mar	Flip-flop and state machine timing	8.1.4	9.2, 13.1		3.5
	Lab 2: Finite state machines				
22-Mar	(Holiday)				
29-Mar	Memory	6.6, 9.1	7.1, 15.1-3		2.6, 5.5
	Data storage				
5-Apr	Memory block combination				
	Datapath elements				5.2.4, 5.5.5
12-Apr	Single-cycle datapath, Microcode				
	Processor architecture				7.1-3
19-Apr	Low-level programming				6.*
	Catch-up / review / practice				
	Test 3: Sequential logic Memory, processors				
26-Apr	Course review (final instruction day)				